

Document Description

This slide deck gathers, for purposes of public exhibition, selected photomicrographs of superconducting microcircuits on the first test chip produced by the ongoing effort at Sandia informally called "BARCS" (Ballistic Asynchronous Reversible Computing with Superconductors). This effort spans two formal projects:

"Asynchronous Ballistic Reversible Computation with Superconducting Josephson Junctions,"

• an internally funded project which ran from 2017-2020.

"Asynchronous Ballistic Reversible Computing with Superconducting Elements,"

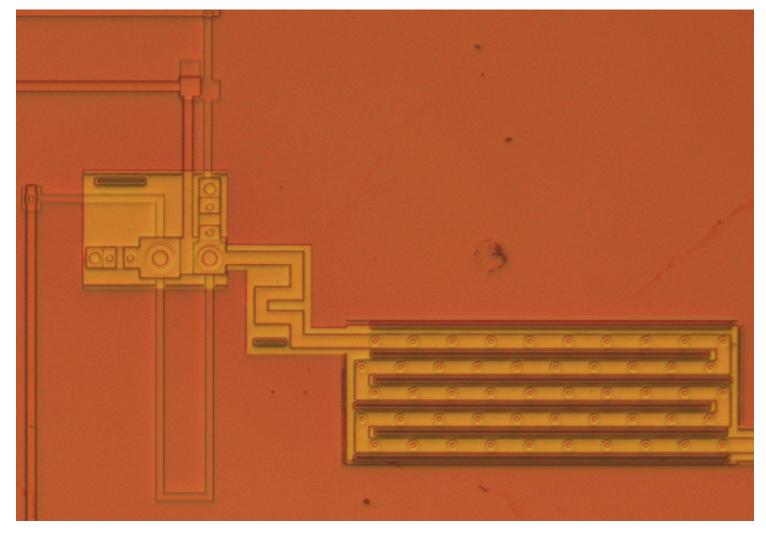
• an externally funded project which started in 2020.

The circuits shown were designed in 2019-2020 using internal funding, and fabricated with support from the external sponsor. Additional information about the goals of this effort, and these particular circuits, can be found in the bibliography on the last slide, and at

http://www.cs.sandia.gov/cr-mpfrank

DC-to-SFQ Converter Feeding dLJJ Ballistic Interconnect

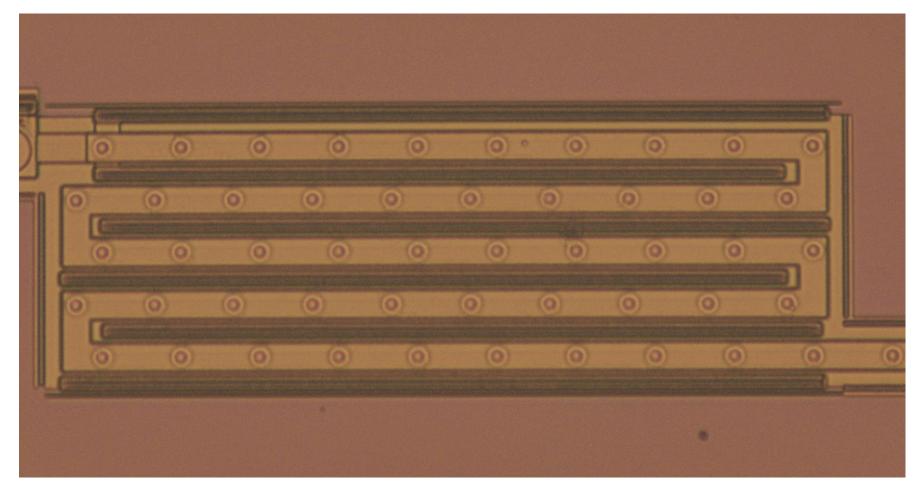




Photomicrograph of a portion of the test circuit for the RM cell. At left is a simple DC-to-SFQ converter circuit designed by Rupert Lewis. This feeds a stripline inductor which broadens the SFQ pulse, matching the pulse width for input to the discrete Long Josephson Junction (dLJJ), the S-shaped structure at lower right, which is folded up in this design for compactness. This delivers the input fluxon to the RM cell (not shown in this image.) Approved for public release, SAND2020-8005 O.

Discretized Long Josephson Junction (dLJJ) Interconnect—A Nonlinear Transmission Line for Flux Soliton Transport

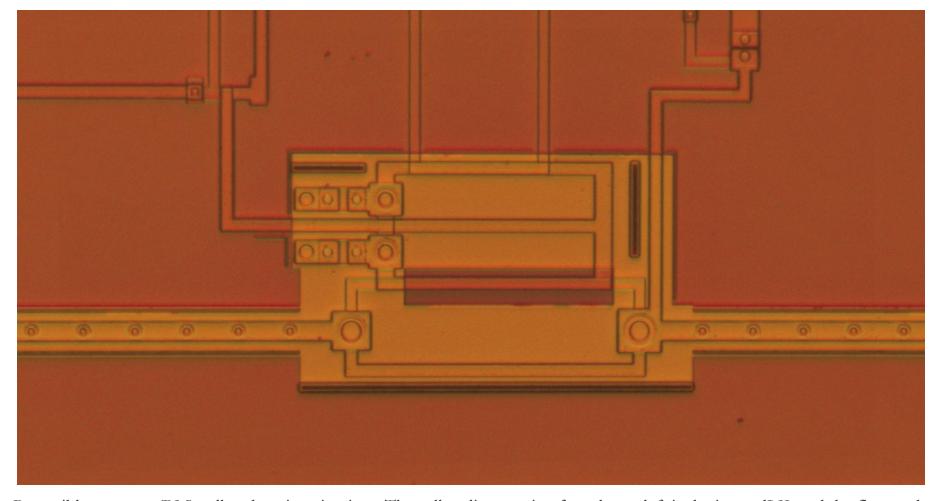




Close-up photomicrograph of a discretized Long Josephson junction (dLJJ) included in our test circuit for the RM cell. (Layout by Nancy Missert.) The small dots are nominally 15 μ A critical current unshunted junctions connecting the upper stripline to a current return stripline underneath. The full structure shown here includes 51 such junctions. The width of the fluxon is approximately 10-11 unit cells, so, about equal to the width of the structure. Approved for public release, SAND2020-8005 O.

Reversible Memory (RM) Cell With Measurement SQUID and Reset Circuit





Reversible memory (RM) cell and testing circuitry. The yellow line coming from lower left is the input dLJJ, and the flattened box shaped structure that it connects to (lower center) is the RM cell itself (storage loop). The "entrance" JJ on its left side is nominally about 75 μ A. The figure-8 structure overlapping the RM cell is a SQUID (superconducting quantum interference device) that is mutually inductively coupled to the RM cell (within the dark cutout area); this is added for purposes of measuring the stored flux. At the right side of the RM cell is a ~100 μ A JJ which may be externally pulsed, which allows any stored flux to be "flushed" out of the cell (and emitted down the LJJ to lower right), providing another method of readout via an SFQ-DC converter (not shown), and also resetting the cell to a null (0 flux) state to prepare it for a new testing sequence. Approved for public release, SAND2020-8005 O.

Bibliography

Frank, Michael P, Rupert M. Lewis, Nancy A. Missert, Karpur Shukla, "Asynchronous Ballistic Reversible Computing using Superconducting Elements," Presentation, ACS BAA Portfolio Review, April 2020.

Frank, Michael P, Rupert M. Lewis, Karpur Shukla, "Implementing the Asynchronous Reversible Computing Paradigm in Josephson Junction Circuits," *Presentation*, 21st Biennial U.S. Workshop on Superconductor Electronics, Devices, Circuits, and Systems, October 2019.

Frank, Michael P, Rupert M. Lewis, Nancy A. Missert, Matthaeus Wolak, Michael David Henry, Erik P. DeBenedictis, "Modeling Asynchronous Ballistic Reversible Computing (ABRC) Primitive Elements Using Superconducting Circuits," Poster, International Superconductive Electronics Conference, July 2019.

Frank, Michael P, <u>"Semi-Automated Design of Functional Elements for a New Approach to Digital Superconducting Electronics: Methodology & Preliminary Results,"</u> *Presentation,* International Superconductive Electronics Conference, July 2019.

Frank, Michael P, Rupert M. Lewis, Nancy A. Missert, Michael David Henry, Matthaeus Wolak, Erik P. DeBenedictis, "Semi-Automated Design of Functional Elements for a New Approach to Digital Superconducting Electronics: Methodology and Preliminary Results," Conference Paper, International Superconductive Electronics Conference, July 2019.

Frank, Michael P, Rupert M. Lewis, Nancy A. Missert, Matthaeus Wolak, Michael David Henry, "Asynchronous Ballistic Reversible Fluxon Logic," *Journal Article*, IEEE Transactions on Applied Superconductivity, Accepted/Published March 2019.

Frank, Michael P, "Improved superconducting logic families (asynchronous, ballistic, reversible, etc.)--a difficult engineering challenge for SCE," Presentation, Applied Superconductivity Conference, November 2018.

Frank, Michael P, Rupert M. Lewis, Nancy A. Missert, Matthaeus Wolak, Michael David Henry, "Asynchronous Ballistic Reversible Fluxon Logic," *Poster*, Applied Superconductivity Conference, October 2018.

Frank, Michael P, "Asynchronous Ballistic Reversible Computing," Presentation, 2nd IEEE International Conference on Rebooting Computing (ICRC 2017), November 2017.

Frank, Michael P, "Asynchronous Ballistic Reversible Computing," Conference Paper, 2nd IEEE International Conference on Rebooting Computing (ICRC 2017), November 2017.